ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 1.852

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

Matlab Simulation of Very High Frequency Resonant Converters for LED Lighting

Avinash.C.M[*1], Sharad Darshan.H.C[2]
[*1] M.tech Student, [2]Asst. Professor, Power Electronics, Dr.AIT, India
cm_avi2@yahoo.co.in

Abstract

This Paper presents a Very High Frequency DC–DC Converters for LED Lighting. As we know that DC-DC Converters are used in converting the unregulated DC input into a controlled DC output at a desired voltage level. It is been observed that from last one decade the focus on green and environmental friendly energy usage has been increased. This has lead to a large increasing in the use of Light Emitting Diodes (LED's) for lighting purpose. The bulbs are quite expensive due to both expensive LEDs and the power converter needed to supply these. Hence there is a strong demand for small, cheap and efficient power converters. In this Paper three different resonant topologies are compared and their usability is discussed.

The proposed Converter for LED lighting is a resonant based high frequency Converter called as SEPIC (Single Ended Primary Inductor Converter) which is advantageous compared to other type of converter topologies which is compared in this paper. The proposed Converter design provides high efficiency over a wide input and output voltage range, up-and-down voltage conversion, small size and excellent transient performance.
Simulation of a 51MHz Converter with 40V input and 15V output are made. The Simulation shows possibility of achieving higher efficiency with a Power MOSFET.

Keywords: MOSFET, SEPIC, Class E Converter, Inverter, Rectifier.

Introduction

During the last decade the focus on green and environment friendly energy usage has been constantly increasing more and more, as a part the usage of Incandescent bulbs, Sodium vapour lamps, Mercury Vapour lamps are been replaced by CFL (Compact Florescent Lamp) and LED (Light Emitting Diode). The bulbs are quite expensive due to both expensive LEDs and the power converter needed to supply these. Due to this there is a strong demand for small, cheap and efficient power converters [35].

It is observed that Switch-Mode Power Supplies (SMPS) are limited by their passive energy storing elements. In Pulse Width Modulated DC-DC and DC-AC Converter topologies the Controllable switches are operated in a switch mode where they are required to turn on and turn off the entire load current during each switching. In Switch mode operation, the switches are subjected to high frequency stress and high frequency power loss that increases linearly with the switching frequency of the PWM. Another significant drawback of the Switch mode DC-DC power supplies is EMI produced due to large di/dt and dv/dt caused by Switched mode operation. As both the physical size and price of this scale with the switching frequency (f_S), increasing f_S into the Very High Frequency band (VHF, 30-300 MHz) will make it possible to achieve higher power density and lower cost. Increasing the switching frequency has several other advantages, which has been discussed. By increasing the operating frequency, the physical size of energy storing elements such as magnetic and capacitive components is also reduced.

High increase in f_S causes several new problems to arise. One of the main problems is the switching loss, which increases linearly with f_S. As f_S increases into the VHF band the switching losses becomes so severe that it will be impossible to cool the switching device and keep the efficiency high. Several researchers [1] have tried to use different types of resonant converters with Zero Voltage Switching (ZVS) and/or Zero Current Switching (ZCS) in order to reduce or ideally eliminate these losses.

It is observed that due to the resonating behaviour of these converters it is however very difficult to control these converters for varying load efficiently. The most efficient way is to use burst mode control to simply Pulse Width Modulate

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 1.852

(PWM) the converter in order to achieve the desired output [2] and [5].

When Converters working for a continuous cycle in open loop these converters will have an almost constant current output for a given input voltage. This is the reason that makes them very well suited for LED applications where it is the current that needs to be controlled. Another advantage of this is, as the output current is constant for a given input voltage the current through the LED will be constant even as the forward voltage changes due to changes in temperature. It is seen that the life time of LED bulbs are limited by the electrolytic capacitors needed, increasing the switching frequency will eliminated this need and hence increase the life time of the bulb.

This paper will give an example of the design of a VHF resonant DC/DC converter used in LED lighting Application. First an appropriate selection of topology is made by comparing different topologies in section II, Secondly the design consideration of proposed converter (SEPIC) is shown in section III. Section IV gives the Simulation and Component selection and design of gate drive circuit is given for the proposed converter. Section V shows the simulated models and its results for the proposed Converter topologies using MATLAB 2013 and finally section VI concludes the paper.

Selection of Topology

In design of resonant DC/DC converters it is very common to split the converter in to two parts; 1) a resonant inverter which converts given DC input voltage into a sinusoidal output current 2) a resonant rectifier that rectifies the AC current to a DC output [3] and [4].

The most commonly used rectifier is the class E rectifier. The main advantage of Class E rectifier is the elimination of switching losses and the reduction in EMI. Other alternative rectifier circuits also exist [1] and [6]. Due to very simple schematic with a single diode the class E rectifier is chosen for these converter topologies.

For the inverter part the Class E type inverter topology have been proposed.

The class E inverter (used in [7] - [3]) shown in Fig. 1 has only a low side switch and is therefore much simpler to drive, however it imposes a huge voltage stress on the switch. As it is observed that the drain of the switch is connected to the input through an inductor, the average drain-source voltage (V_{DS}) of the switch has to be equal to the input voltage. Even if V_{DS} is assumed constant when the switch is closed, the peak switch voltage will be two times V_{IN} for a duty cycle of 50 %. In reality the voltage across the switch is more like a half wave rectified sine wave in order to achieve Z_{VS}, which result in a peak voltage of 3.56 times V_{IN} [8].

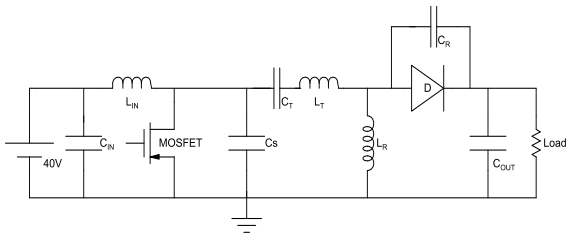

Fig. 1. Schematic of Class E Inverter and Class E Rectifier.

In other words the maximum Switch Utilization Ratio (Switch Utilization Ratio is defined as the rate of output power P_o to the product of peak switch voltage and the peak switch current). It is shown in the literature that the peak switch current is approximately $3I_d$ and peak switch voltage is approximately $3.5V_d$ [9].

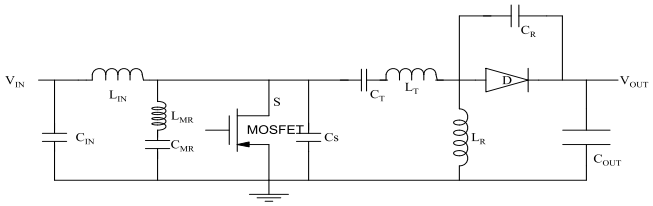

Fig.1a. Schematic of Class EF$_2$ Inverter and Class E Rectifier.

In order to reduce this huge peak voltage the class EF_2 (or Φ_2), which is a hybrid between the class E and class F_2, has been developed

According to these the Class F and its variants are of same radio frequency power amplifier, uses resonant harmonic peaking of the input or the output network [4], [10]-[17] to reduce the peak voltage the switch. A switch mode variant of Class F inverter that can be made highly efficient is called Class φ Inverter. In this Class EF_2 topology it introduces an extra resonant circuit (C_{MR} and L_{MR} in Fig. 1a) across the drain and source of the switch with a zero at the second harmonic of f_S. If tuned correctly this adds the third harmonic of f_S on top of the sine wave seen with the class E. This results in a trapezoidal waveform across the switch. This reduces the peak voltage a bit, but increases complexity and results in additional losses due to large AC current at three times f_S.

The SEPIC converter shown in Fig. 2 is similar to that of the schematic of Class E inverter and with L_T removed. However the waveforms are

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 1.852

different, as this converter cannot be split into an inverter and a rectifier. The changed waveforms results in a much smaller input inductor than needed for the class E inverter, thus the achievable power density is higher due to fewer and smaller inductors.

Based on the analysis of the four converter topologies the SEPIC converter was chosen as it gives the highest power density and lowest cost.

Design of Proposed Resonant Converter (Sepic Converter)

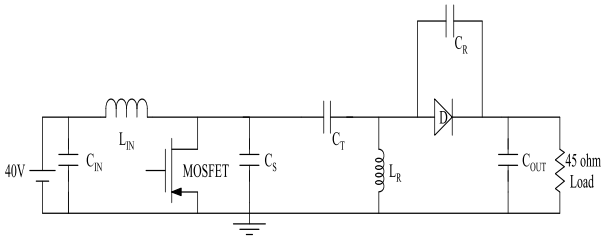

Fig. 2. Schematic of Proposed SEPIC Converter.

Fig. 2 shows the power stage of the proposed converter. The topology used here has some topological similarities with both the conventional SEPIC converter [18] and with the multiresonant SEPIC converter proposed in [19]. However, the detailed component placement and sizing, operating characteristics, and control approach are all very different from previous designs.

First, consider the circuit topology. The conventional SEPIC converter has two bulk (ac choke) inductors and yields hard switching of the switch and diode. Thus, in the conventional quasi-resonant SEPIC converter, L_F is a choke inductor, selected to provide nearly constant current over a switching cycle. The multiresonant SEPIC [19] utilizes similar bulk inductors, but explicitly introduces capacitances in parallel with the switch and diode along with a resonant inductor in series with the coupling capacitor C_S to achieve zero-voltage soft switching of the switch and diode. The design introduced here also explicitly utilizes capacitances in parallel with the switch and diode. However, in contrast to previous resonant SEPIC designs [20], [19], the design here has no bulk inductors. Rather, it uses only two resonant inductors: one inductor L_F resonates with the net switch capacitance, C_{OSS} +C_S, for resonant inversion, while the other inductor L_R resonates with the rectifier capacitance C_{EX2} for resonant rectification. This design method leads to reduced magnetic component count, along with greatly increased response speed.

A further major difference between the converter proposed here and previous resonant SEPIC converters relates to control. The conventional resonant SEPIC converter regulates the out-put voltage by keeping the on-time pulse fixed while varying the OFF time duration, leading to variable-frequency, variable-duty-ratio operation. Unlike conventional designs which used variable-frequency control to regulate the output [20], [19], the design here operates at fixed switching frequency and duty ratio. (As will be discussed in Section IV, output control is instead achieved through ON/OFF control, in which the entire converter is modulated ON and OFF at a modulation frequency that is far below the switching frequency [21]–[28].) Operation at a fixed frequency and duty ratio enables the elimination of bulk magnetic components (described previously) and facilitates the use of highly efficient sinusoidal resonant gating (described in Section IV). Moreover, it enables zero-voltage soft switching to be maintained over wide input and output voltage ranges, and eliminates the variation in device stress with converter load that occurs in many resonant designs [20], [19].

Operation of this converter can be understood as a linking of two subsystems: a resonant inverter and a resonant rectifier. The design procedure for the proposed topology involves designing the rectifier and inverter individually, coupling the inverter and rectifier together, then retuning as necessary to account for non-linear interactions between the inverter and rectifier. We discuss these steps in the following sections.

Rectifier Design

The design procedure of a full dc–dc converter starts with the rectifier. In the proposed converter the rectifier utilizes a resonant tank comprising a resonant inductor L_R and a capacitor C_R along with an additional parasitic junction capacitance from diode D. In designing of a rectifier circuit we are assuming that the circuit is driven by a sinusoidal current source I_N at a given output voltage V_{OUT}. For a desired output power level and operating frequency, the rectifier is tuned to appear resistive in a describing function sense by adjusting C_R and L_R .That is we adjust C_R and L_R such that the fundamental component of V_R is in phase with the drive waveform I_{IN} to ensure the desired power is delivered through the rectifier.

It can also be that the equivalent rectifier impedance at the operating frequency is calculated as a complex ratio Z_{EQV}= V_{R1}/I_{IN} where V_{R1} is the fundamental of V_R (i.e., voltage across the inductor L_R). This equivalent impedance can be used in the

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 1.852

place of the rectifier for designing the resonant inverter assuming that the majority of the output power delivered to the load transferred through the fundamental.

In the rectifier design for SEPIC converter, as the value of L_R and C_R are changed, output power level and the phase relationship between V_R and I_{IN} changes. It is also seen that as the phase difference between V_R and I_{IN} increases the losses due to reactive current rise, reducing the output power and overall efficiency of the rectifier.

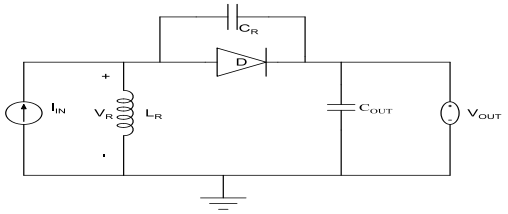

Fig. 3. Circuit model for tuning of the resonant rectifier.

The following design example of a 4-W rectifier at a nominal output voltage of 7 V illustrates the tuning procedure described earlier. The rectifier uses a commercial Schottky diode DFLS230L (having an approximate capacitance of 70 pF) and is driven by a sinusoidal current source I_{IN} with an amplitude of 0.7 A. The value of L_R of the resonant rectifier is selected in conjunction with C_R so that the fundamental rectifier input voltage V_R is in phase with rectifier input current I_{IN}. Fig. 4 shows the input current and voltage of a resonant rectifier (like the one in Fig. 2) simulated using PSPICE. For the simulation shown, L_R = 118nH, C_R = 150 pF, V_{OUT} = 7V, and the sinusoidal input current I_{IN} = 0.7A at a frequency of 20MHz. The average power delivered to the load under these conditions is 4.12W. In Fig. 4, the fundamental component of the input voltage and the current are in phase resulting in a rectifier with an equivalent resistance (at the fundamental) of approximately 17.14Ω. As the values of L_R and C_R are changed, output power level and the phase relationship between V_R and I_{IN} change. As the phase difference between V_R and I_{IN} increases, the losses due to reactive currents rise, reducing the output power and the overall efficiency of the rectifier, as shown in Table I.

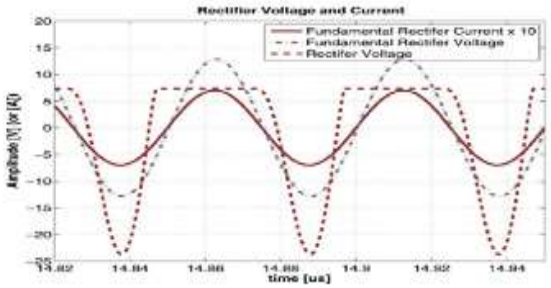

Fig. 4. Fundamentals of rectifier voltage V_R and current I_{IN} of the resonant rectifier of Fig. 2 tuned to look resistive at an operating frequency of 20 MHz. Simulation is for a rectifier built with a DFLS230L Schottky diode, L_R = 118nH, C_R = 150 pF, and V_{OUT} = 7V

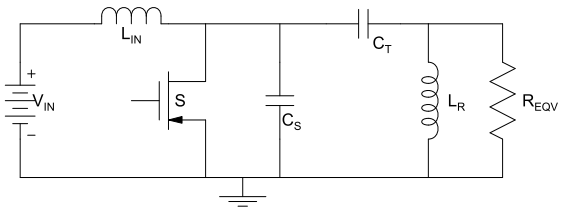

Fig. 5. Resonant inverter including a matching circuit and equivalent load resistance. This circuit model is used for tuning the inverter.

Table I: Tuned and Detuned Rectifier Component Values

L_R	90nH	118nH	118nH
C_{EX2}	150pf	50pf	150pf
$\|Z_{EQV}\|$	18.07Ω	19.08Ω	18.12Ω
$\angle Z_{EQV}$	36.9^0	47.9^0	0
POUT	2.28W	2.97W	4.12W
EFFICIENCY	89.6%	90.6%	91.4%

Inverter Design

Consider the inverter network of Fig. 5, which includes impedance matching from the inverter to the equivalent rectifier impedance. In design of inverter, the design begins with tuning by selecting approximate matching circuits.

(In figure 3 and 5 i.e., rectifier and inverter circuits L_S and L_R is combined (parallel combination of L_S and $L_{R\ is}$ named as L_R in the SEPIC converter)). In designing of inverter circuit that most power transferred through the fundamental, the maximum equivalent resistance R_{MAX} needed to deliver an output power level of P_{OUT} with a fundamental voltage at the MOSFET drain is V_{DS} which can be calculated from $R_{MAX} = V^2_{DS}/(2*P_{OUT})$ where R_{MAX} is the transformed resistance loading the drain to source port of the inverter. (But in a SEPIC converter the V_{DS} of the drain voltage is not exactly $1.6*V_{IN}$;

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 1.852

the effects of which can be addressed by adjusting output power when coupling the inverter and rectifier together).

When the rectifier equivalent resistance R_{EQV} is higher than the value R_{MAX} to meet the output power requirement, a matching network consisting of L_S and C_S is required to transform the load impedance to a lower value [22], [30], [31]. The approximate transformation ratio can be obtained as R_{MAX}/R_{EQ}. One possible starting point for selecting the component values for L_S and C_S is to design a matching network such that a transformation ratio R_{MAX}/R_{EQV} occurs at the desired operating frequency. Additional minor adjustments on these component values may be done later in conjunction with tuning C_F and L_F with a simulation tool (e.g., PSPICE) to achieve a resulting drain-to-source switching waveform V_{DS} that has Zero-Voltage Switching (ZVS) and zero dv/dt at turn ON. In practice, the resonance of L_S and C_S can be set to be exactly at the switching frequency, or slightly above or below the resonant frequency, all of which are typically viable and will lead to a working design. In a given application, one tuning may result in more achievable component values and, therefore, may be more favorable compared to the others. Once matching network components have been selected, inductance L_S may be absorbed into the rectifier inductance L_R.

The input resonant network, comprising L_F and C_F, largely shapes the frequency at which the drain waveform rings up and down. For an inverter operating at a 50% duty ratio, one possible starting point for L_F is to tune the input resonant network such that its resonance frequency is at twice the switching frequency, as in (1). This tuning selection is similar to that of the "second harmonic" class E inverter in [32] and [33]:

$$L_F = 1/16\pi^2 f^2_{SW} C_F \qquad (1)$$

Note that the capacitor C_F includes the parasitic capacitance of the semiconductor switch and possibly an external capacitor C_S. In some applications, where the packaging inductance of the semiconductor switch is significant, selecting C_F to be solely provided by the device capacitance may be a good choice, because it prevents waveform distortion caused by additional ringing between the external capacitance and the package inductance. In other cases, where the circulating current is significant, it is a better choice to add additional high-Q ceramic capacitance in parallel with the lossy device parasitic capacitance to reduce the circulating current loss. One starting point for C_F is to assume that it is comprised solely of parasitic capacitance of the semiconductor switch, allowing an initial value of L_F to be calculated. Since L_F significantly impacts the transient response speed, a small L_F is generally preferred. If the starting point of C_F leads to too large a value of L_F, additional parallel capacitance C_{EX} may be added until the value of L_F is in the desired range.

Once the initial values of L_F, C_F, L_S, and C_S are determined from the aforementioned procedure, additional tuning can be made via minor adjustments of the component values along with the duty ratio until the resulting drain-to-source switching waveform V_{DS} achieves ZVS and zero dv/dt turn ON, the so-called class E switching waveform.

Using the equivalent resistance $R_{EQV} = 17.14\ \Omega$ from the rectifier design discussed previously, a 20-MHz inverter utilizing two commercial vertical MOSFETs SPN1443 in parallel can be designed in the following manner: a matching network which transforms the equivalent rectifier impedance from 17.14 to 4 Ω at about the operating frequency is required in order to deliver 4W at an input voltage of 3.6V. The component values for such a matching network are L_S = 76nH and C_S = 1120pF. If C_F is to be comprised solely of the parasitic capacitance of SPN1443 (about 160 pF), the resulting L_F is about 141nH, a condition which deteriorates the transient response speed and overall closed-loop efficiency. In this design, it is determined through time-domain simulations that it is desirable to add additional high-Q ceramic capacitance in parallel with the lossy device parasitic capacitance to reduce the overall loss as well as the component value (and size) of the input inductor L_F. A starting value for L_F is chosen to be 22nH (so that the inductance is small enough to allow for fast transient response and large enough to not be significantly affected by low-Q board parasitic inductance), resulting in an external capacitor C_S of 550 pF at a 50% duty ratio.

C. DC–DC Retuning

An entire converter design may be accomplished by connecting the tuned inverter to the resonant rectifier. When the inverter and rectifier are connected, the circuit waveforms and the output power level may be slightly different than that predicted by the inverter loaded with the equivalent impedance, due to the non-linear interaction between the inverter/matching network with the rectifier. Minor additional tuning may thus be required to achieve ZVS and the required power level. The final component values for a complete converter using the example rectifier and inverter design described in this section will be presented in Section V. A complete

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 1.852

discussion of the tuning methodology for these components is found in [34].

Fig. 7 shows the idealized drain and rectifier voltage wave-forms for the proposed design over a range of input voltages using the techniques outlined in previous subsections (the component values are included in the description of Fig. 7).

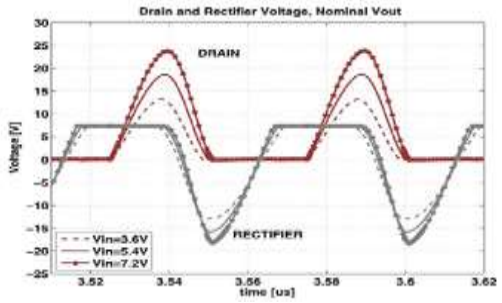

Fig. 7. Simulated drain V_{DS} and rectifier V_R voltages for a 20-MHz converter operating with V_{OUT} = 7 V, L_F = 22nH, C_S = 780pF, C_R = 100pF, C_T = 1270pF, and L_P = 41nH. Inductor Q of 70 and capacitor Q of 3000 is assumed. Two MOSFETs and a Diode are used.

It can be seen that zero-voltage soft switching is achieved at fixed frequency and duty ratio across a wide range of input voltages. In addition, while developing the design required tuning of the selected circuit component values, this tuning needed only to be performed once. The converter performance was found to be repeatable across several prototypes. Moreover, the converter is tolerant of the device nonlinear capacitance variation with input voltage over the entire operating range.

Simulation and Component Selection

A model of a resonant SEPIC converter has been set up in spice based on the tuning procedure explained in [34]. The converter is designed to have the specifications given in table II. The converter will be used to supply a string of LEDs with a combined forward voltage drop of 12-15 V, depending on temperature and power level.

Table IIDesign Specifications

Specification	Symbol	Value
Input voltage	V_{IN}	40 V
Output power	P_{OUT}	5 W
Output Voltage	V_{OUT}	15 V
Switching frequency	f_S	51 MHz

From the simulations it is seen that the MOSFET should have a break down voltage of at least 100V (see Figure 11), however if the duty cycle is adjusted closer to 50 % the peak voltage will get close to 143 V (3.56 times the input voltage as for the class E). For this reason it was decided to build the prototype around an IRF5802 MOSFET from International Rectifier. The MOSFET has a break down voltage of 150 V and small parasitic capacitances compared to its competitors.

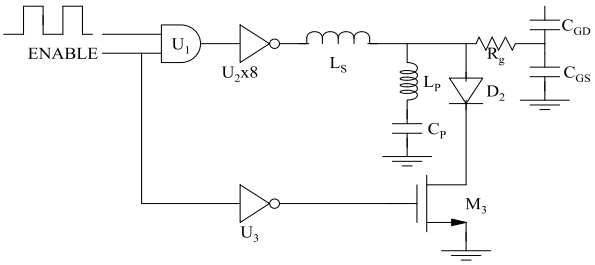

Fig. 8. Resonant sinusoidal gate drive circuit with MOSFET gate model.

The peak voltage is slightly above 40 V (see Figure 9 where V_{AC} is anode-cathode voltage) and a MBR0540 40 V Schottky diode has therefore been selected. C_R needs to be 105 pF which is more than the parasitic capacitance of a single diode (35 pF), thus it is necessary either to add a 70 pF capacitor or use three diodes in parallel. The last solution has the benefit of sharing the current between the three devices. As the forward voltage drop of the diodes increases with the current running through them, this will lead to reduced losses and this solution was therefore selected.

The inductors are all square air core inductors (1515SQ-68N, 1515SQ-82N and 2222SQ-161) as they have a fairly high Q factor and are available off the shelf which ease implementation. The CT capacitor is implemented with 4 parallel capacitors as it was found that this increased the efficiency of the converter with 1-2 % compared to using a single capacitor of the same value. For the input and output capacitors standard 1µF X7R capacitors was selected.

Fig. 8 shows the gate drive circuit for the proposed converter [36].

Matlab Model and Simulation Results

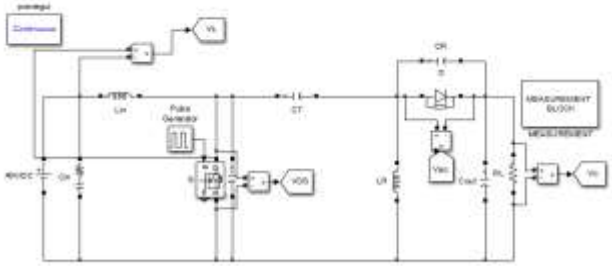

Fig 9. Proposed SEPIC Converter MATLAB model

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 1.852

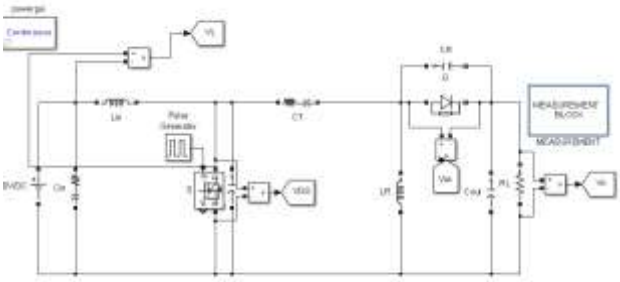

Fig 10: CLASS E resonant converters MATLAB Model

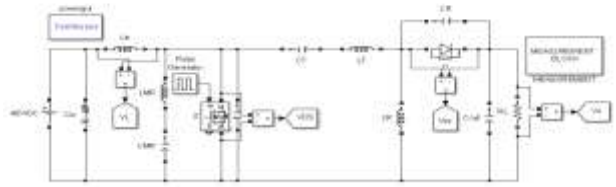

Fig 10. a: CLASS EF_2 resonant converters MATLAB Model

Figures (9,10,10.a) shows the proposed SEPIC Converter CLASS E and CLASS EF_2 Converters MATLAB models respectively. The designed Converter is operated with a 40V regulated input DC supply and output obtained is 15V DC. In the proposed Converter shown above in figure9, the inverter design begins with the approximate matching components (i.e., selection of the L_{IN}, C_F and C_T). Similarly L_R and C_R are responsible for resonant rectification. Results of the proposed Converter are obtained according to the design considerations made. In the above figures (9,10,10.a) measurement box includes the measurement of output results of different parameters.

Design Specifications And Component Details Of Proposed Converter

SL.NO.	COMPONENT	SIMULATED	TYPE
1	C_{IN}	1μF	Capacitor
2	L_{IN}	160nF	Inductor
3	S		P Channel MOSFET
4	C_F	22pF	Capacitor
5	L_R	82nF	Inductor
6	C_T	40pF	Capacitor
7	D		Schottky Diode
8	C_R	105pF	Capacitor
9	C_{OUT}	1μF	Capacitor

Result Obtained For The Proposed Converter, Drain To Source Voltage (V_{DS})

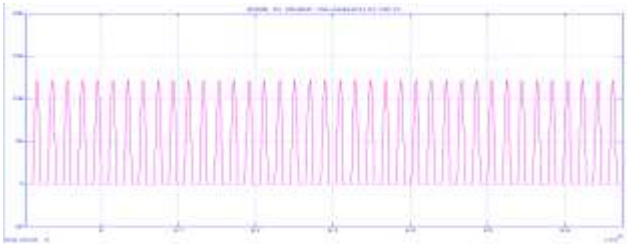

Fig.11 . Drain to Source voltage (V_{DS}) across the terminals of MOSFET of a SEPIC Converter

In the above figure (11), according to simulation output it is seen that the MOSFET will have a break down voltage of at least 100V. However if the duty cycle is made 50% then the peak voltage will be nearly close t0 143V (i.e., 3.6 times the input of the input voltage).

ANODE TO CATHODE VOLTAGE (V_{AC})

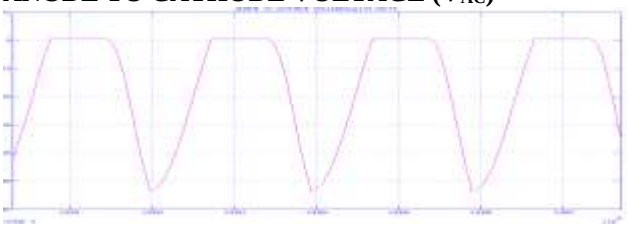

Fig. 12. Anode to Cathode voltage (V_{AC}) across Diode in rectifier circuit of A SEPIC ConverterFigure (12) shows the output voltage across Diode D. It is

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 1.852

observed that the peak voltage V_{AC} is slightly above the input voltage (V_{IN}).

OUTPUT VOLTAGE ACROSS THE LOAD (V_{OUT})

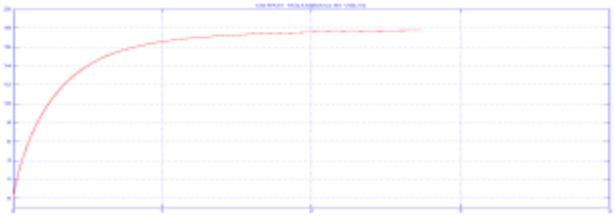

Fig. 13.a. Output voltage (V_{OUT}) across load resistor R_L in Proposed SEPIC Converter

Fig. 13.a shows the output voltage across the load resistor R_L for the proposed converter. Here the output load resistor is selected with a value of 45Ω according to the calculations based on output power and output voltage [TABLE II]. It is observed that the output voltage is nearly constant after attaining a maximum voltage of 18V.

Conclusion

This paper has covered three different converter topologies. From the simulation, it is observed that, compared to the CLASS E and CLASS EF_2 Converter, the SEPIC converter has response time faster due to the absence of bulk inductor. Efficiency is higher compared to the conventional Converter topologies.

References

[1] *W. C. Bowman, J. F. Balicki et al., A resonant DC-to-DC converter operating at 22 megahertz, in IEEE 1988 Applied Power Electronics Conference, 1988, pp. 3-11 July 1993.*

[2] *Very-High-Frequency Resonant Boost Converters Robert C. N. Pilawa-Podgurski,, Anthony D. Sagneri, Juan M. Rivas, David I. Anderson, and David J. Perreault, IEEE Transactions on Power Electronics, Vol. 24, No. 6, June 2009.*

[3] *Marian K. Kazimierczuk and Jacek Jozwik, Resonant dc/dc Converter with Class-E Inverter and Class-E Rectifier, in IEEE Transactions on Industrial Electronics, vol. 36, no. 4, pp. 468-478, Nov 1989.*

[4] *Juan M. Rivas, Olivia Leitermann et al., A Very High Frequency dc-dc Converter Based on a Class ϕ2 Resonant Inverter, in IEEE 2008 Power Electronics Specialists Conference, 2008, pp.1657-1666.*

[5] *James R. Warren, III, Kathryn Anne Rosowski and David J. Perreault Transistor Selection and Design of a VHF DC-DC Power Converter, in IEEE Transactions on Power Electronics, vol. 23, no. 1, pp. 27-37, Jan. 2008.*

[6] *David C. Hamill, Class DE Inverters and Rectifiers for DC-DC Conver-sion, in IEEE 1996 Power Electronics Specialists Conference, 1996, pp. 854-860.*

[7] *Toke M. Andersen, A VHF Class E DC-DC Converter with Self-Oscillating Gate Driver, in IEEE 2011 Applied Power Electronics Conference, 2011, pp. 885-891.*

[8] *Analysis and Design of Class-E3F and Transmission-Line Class-E3F2 Power AmplifiersMury Thian and Vincent F. Fusco, Fellow, IEEE.*

[9] *Power Electronics, text book, Mohan Undel and Robbins.*

[10] *V. Tyler, "A new high-efficiency high-power amplifier," The Marconi Rev., vol. 21, no. 130, pp. 96–109, 3rd qtr. 1958.*

[11] *S. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, "The class E=F family of ZVS switching amplifiers," IEEE Trans. Microw. Theory Tech., vol.51, no. 6, pp. 1677–1690, Jun. 2003.*

[12] *F. H. Raab, "Class-F power amplifiers with maximally flatwaveforms," IEEE Trans. Microw. Theory Tech., vol. 45, no. 11, pp. 2007–2012, Nov. 1997.*

[13] *K. Honjo, "A simple circuit synthesis method for microwave class-F ultra-high-efficiency amplifiers with reactance-compensation circuits," Solid-State Electron., pp. 1477–1482, 2000.*

[14] *F. H. Raab, "Maximum efficiency and output of class-F power amplifiers," IEEE Trans. Microw. Theory Tech., vol. 49, no. 6, pt. 2, pp. 1162–1166, June 2001.*

[15] *A. Grebennikov, "Effective circuit design techniques to increase MOSFET power amplifier efficiency," Microw. J., pp. 64–72, July2000.*

[16] *A. Grebennikov, "Circuit design techniques for high efficiency class-F amplifiers," in Proc. IEEE Microwave Theory and Techniques Symp., 2000, pp. 771–774.*

[17] *A. Grebennikov, RF and Microwave Power Amplifer Design. New York: Mc Graw-Hill, 2005, ch. 7.*

[18] *R. Erickson and D. Maksimovic,´ Fundamentals of Power Electronics, Norwell, MA: Kluwer, 2000.*

[19] *W. Tabisz and F. Lee, "Zero-voltage-switching multiresonant technique: A novel approach to*

improve performance of high-frequency quasi-resonant converters," IEEE Trans. Power Electron., vol. 4, no. 4, pp. 450–458, Oct. 1989.

[20] F. Lee, "High-frequency quasi-resonant converter technologies," in Proc. IEEE Conf., Apr. 1988, vol. 76, no. 4, pp. 377–390.

[21] Y. Lee and Y. Cheng, "A 580 KHz switching regulator using on-off con-trol," J. Inst. Electron. Radio Eng., vol. 57, no. 5, pp. 221–226, Sep./Oct. 1987.

[22] J. Rivas, D. Jackson, O. Leitermann, A. Sagneri, Y. Han, and D. Per-reault, "Design considerations for very high frequency dc-dc converters," in Proc. 37th IEEE Power Electron. Spec. Conf., Jun.18–22, 2006, pp. 1–11.

[23] J. Rivas, R. Wahby, J. Shafran, and D. Perreault, "New architectures for radio-frequency dc/dc power conversion," IEEE Trans. Power Electron., vol. 21, no. 2, pp. 380–393, Mar. 2006.

[24] R. C. Pilawa-Podgurski, A. D. Sagneri, J. M. Rivas, D. I. Anderson, and J. Perreault, "Very high frequency resonant boost converters," in Proc. Power Electron. Spec. Conf., Jun. 2007, pp. 2718–2724.

[25] J. M. Rivas, "Radio frequency dc-dc power conversion," Ph.D. disserta-tion, Dept. Elect. Eng. Comput. Sci., Massachusetts Institute of Technol-ogy (MIT), Cambridge, Sep. 2006.

[26] A. D. Sagneri, "Design of a very high frequency dc-dc boost converter," M.S. thesis, Dept. Electr. Eng. Comput. Sci., Massachusetts Institute of Technology (MIT), Cambridge, Feb. 2007.

[27] J. Hu, A. D. Sagneri, J. M. Rivas, S. M. Davis, and D. J. Perreault, "High frequency resonant sepic converter with wide input and output voltage ranges," in Proc. IEEE Power Electron. Spec. Conf., Jun. 2008, pp. 1397– 1406.

[28] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Lietermann, R. Pilawa, A. Sagneri, and C. Sullivan, "Opportunity and challenges in very high frequency power conversion," in Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo., 2009, pp. 1–14.

[29] N. O. Sokal, "Class-E RF Power Amplifiers," QEX Mag., pp. 9–20, Jan./Feb. 2001.

[30] W. Everitt and G. Anner, Communications Engineering, 3rd ed. New York: McGraw-Hill, 1956.

[31] Y. Han and D. J. Perreault, "Analysis and design of high efficiency match-ing networks," IEEE Trans. Power Electron., vol. 21, no. 5, pp. 1484– 1491, Sep. 2006.

[32] H. Koizumi, M. Iwadare, and S. Mori, "Class E 2 dc/dc converter with second harmonic resonant class E inverter and class E rectifier," in Proc. 3rd Annu. Appl. Power Electron. Conf., 1994, pp. 1012–1018

[33] M. Iwadare, S. Mori, and K. Ikeda, "Even harmonic resonant class E tuned and power amplifier without RF choke," Electron. Commun. Jpn., vol. 79, no. 1, pp. 23–30, Jan. 1996.

[34] J. Hu, "Design of a low-voltage low-power dc-dc vhf converter", M.S. the-sis, Dept. Elect. Eng. Comput. Sci., Massachusetts Institute of Technology (MIT), Cambridge, 2008.

[35] Very High Frequency Resonant DC/DC Convertersfor LED Lighting Mickey P. Madsen, Arnold Knott*, Michael A. E. Andersen.*

[36] Jingying Hu, , Anthony D. Sagneri, Juan M. Rivas, Yehui Han, Seth M. Davis, and David J. Perreault, "High-Frequency Resonant SEPIC Converter With Wide Input and Output Voltage Ranges", IEEE Transactions on Power Electronics, Vol. 27, No. 1, January 2012.